REMARKS

The Office Action mailed July 23, 2007, has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Subject Matter Indicated Allowed or Allowable

Applicants are grateful for the indication of allowability of claims 4, 5, 7 and 9-12, subject to their amendment to include the limitations of the base and intervening claims. As explained below, applicants believe that the base claim (Claim 1) is allowable on its merits and the amendment of claims 4, 5, 7 and 9-12 to incorporate its limitations is unnecessary.

Rejection(s) Under 35 U.S.C. § 103 (a)

Claims 1-3 and 8 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bell (U.S. pat. no. 6,876,239) in view of Staszewski et al. (U.S. pub. no. 2002/0033737). Claim 1, from which claims 2-3 and 8 depend, has been amended to state that "the number of delay cells seen by the phase/frequency detector being able to change at each tick of the clock signal (H)." This feature, supported for example on page 6, lines 13-15 of the description, is not disclosed or suggested by Bell or Staszewski, considered singularly or in combination.

As previously argued, in Bell, the COMMAND_SET signal which controls the multiplexer 130 changes only when it is desired to modify the working mode of the memory. Furthermore, after a change of the COMMAND_SET signal, several XCLK clock cycles are necessary for the delay-locked loop (DLL) to be clamped—that is, for the delay of each DELAY STAGE to be established. Unlike the DLL of Claim 1, the Bell DLL does not allow the delay of each DELAY STAGE to be quickly modified. The ability to make the delay of each DELAY STAGE quickly modifiable allows obtaining, at a DELAY STAGE output, a desired delay average value that can progressively change.

With respect to Staszewski, it will be appreciated that that patent relates to phase-locked loops (PLLs) and digitally-controlled oscillators (DCOs), not to delay-locked loops (DLLs). FIG. 15 in particular, to which the Office Action makes reference, relates to a DCO and the circuit therein is intended to solve spurious tones problems that are peculiar to DCOs. In FIG. 15, the

shift register 1306 does not constitute a line of delay cells as claimed in Claim 1 of the present application, and the phase comparator 1504 does not receive the input signal of the delay chain. Moreover, the delay duration of a register in FIG. 15 is a function of the CKVD clock, and not of the signal output from the phase comparator.

The presently claimed invention is not disclosed or suggested by Staszewski, and provides various advantages, such as the ability to generate a delayed clock signal having a delay that is easily and economically adjustable, and to generate a delayed clock signal which is devoid of any frequency step or rough variation.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-1698.

Respectfully submitted,
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